UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,031	07/11/2003	Hiroshi Shirota	009683-475	2708

7590 10/16/2007

BURNS, DOANE, SWECKER &
MATHIS, L.L.P
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/617,031	SHIROTA, HIROSHI	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 – 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "said clock signal" in Lines 3, 5 and 7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Ramamurthy et al (US 5,787,114).

Ramamurthy teaches of a communication apparatus, comprising: a communication node (#6, Fig.3) and a test communication node (#7, Fig.7) capable of transmitting and receiving a signal between other said communication apparatus (Fig.2); a transmitter (#5, Fig.1) converting received transmit data into a transmit signal and outputting it to said communication node (#11, Fig.3)(Col 6, Lines 64 – 67 to Col 7, Lines 1 – 15); a receiver converting a receive signal that is received at a receive node and outputting the converted receive signal as receive data (#12, Fig.3, Col 7, Lines 1 – 15) ; and a signal switch selectively forming a signal path between one of said communication node and said test communication node, and said receive node (#21, Fig.3); wherein in a first test mode (LoopbackN, #19, Fig.3), a signal path is formed between said communication node (#6, Fig.3) of said communication apparatus and said test communication node (#7, Fig.7) of said other communication apparatus, as well as between said test communication node of said communication apparatus and said communication node (#6, Fig.3) of said other communication apparatus, and wherein within each of said communication apparatus and said other communication apparatus, said signal switch forms a signal path between said test communication node (#7, Fig.7) and said receive node (Col 6, Lines 64 – 67 to Col 7, Lines 1 – 58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 2, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enam et al. (US Pub 2002/0097682) in view of Anderson et al (US 5,793,822).

Re claim 1, Enam teaches of a communication apparatus, comprising: a transmitter (Fig.3A) including an encoder circuit (MUX, #384, Fig.3A) for converting transmit data (TPDAT, parallel data) into a transmit signal (TSDAT, serial data) synchronizing to a transmit clock (#362)(Paragraphs 0059 and 0060); a receiver

(Fig.3B) including a decoder circuit (#306 and #310) for converting a receive signal (RSDAT, serial data, Fig.3B) into receive data (RPDAT, parallel data) synchronizing to a receive clock (REFCLK, Fig.3B, Fig.3A) (paragraphs 0059, 0063 – 0065); and a clock supply select circuit (#386, Fig.3A) controlling a supply of said transmit clock and said receive clock to said transmitter and said receiver, said clock supply select circuit including a clock generate circuit generating an internal clock signal (Paragraph 0065), and a clock circuit generating a clock signal (#326, Fig.3A, 3B) based on said internal clock of reference (REFCLK), wherein in a normal operation mode, said clock supply select circuit supplies said internal clock signal as each of said transmit clock and said receive clock in common (REFCLK, REFCLK always used in the receiver circuit), and in a loopback operation mode (LLB, #386), said clock supply select circuit supplies said internal clock signal as one of said transmit clock and said receive clock and supplies said modulate clock signal as the other of said transmit clock and said receive clock (Abstract and Paragraphs 0073 – 0078). However, Enam does not teach of a clock modulating circuit that introduces jitter into the internal clock of reference.

Anderson teaches of a circuit for testing jitter tolerance of a receiver. The circuit includes a jitter injection circuit that has an output connected to an input in a phase-locked loop circuit. The jitter injection circuit generates an output signal in response to an application of an input signal. The phase-locked loop circuit has an output that generates a clock signal, wherein the clock signal may be altered by the output signal from the jitter injection circuit. The clock signal from the phase-locked loop circuit controls transmission of data at the transmitter. Alteration of the clock signal caused by

the jitter injection circuit alters the manner in which the transmitter transmits data (Abstract, #13, Fig.5, Col 4, Lines 34 – 67 to Col 5, Lines 1 – 30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have introduced jitter into the signal so as to monitor the device response and the tolerance of the receiver line to jitter that can be independently tested.

Re claim 2, Enam teaches of said clock supply select circuit includes a clock switch (#386, Fig.3A) provided corresponding to said transmitter, wherein said clock switch supplies to said transmitter, in said normal operation mode, said internal clock signal as said transmit clock, and in said loopback operation mode, said modulate clock signal as said transmit clock, and wherein said clock supply select circuit supplies to said receiver, in each of said normal operation mode and said loopback operation mode, said internal clock signal as said receive clock (Abstract and Paragraphs 0073 - 0077).

Re claim 5, Enam and Anderson teach all the limitations of claim 1. However, Enam does not teach of a data compare circuit.

Anderson teaches of the transmitter connected to a receiver using a transmission medium. The transmitted data is compared to the received data to determine whether

errors have occurred in response to an alteration of the transmission of data caused by the jitter injection circuit (Col 2, Lines 7 – 11).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have compared the transmitted data with the received data so as to determine whether any errors have occurred in response to an alteration of the transmission of data caused by the jitter injection circuit.

Re claim 7, Enam and Anderson teach all the limitations of claim 1. However, Enam does not teach of differential transmission medium and a signal switch bypassing the differential medium.

Anderson teaches of said transmitter further including a differential driver (#61, Fig.5) converting said transmit signal of a single-end signal into a differential signal to be output, and wherein said receiver further includes a differential receiver (#61, Fig.5) converting a received differential signal into said receive signal of a single-end signal; said communication apparatus further comprising a signal switch (MUX, #55) forming as necessary, in said loopback operation mode, a signal path bypassing said differential driver and said differential receiver for passing said transmit signal output from said encoder circuit directly as said receive signal (Fig. 5. Col 4, Lines 34 – 67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a differential driver in order to achieve cabled

communications and a switch to internally bypass the differential driver and set the system into a loopback mode.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enam et al in view of Anderson et al and further in view of Mak et al. (US 6,885,209).

Re claim 3, Enam and Anderson teach all the limitations of claim 1 except of the clock switch supplies to said receiver, in said normal operation mode, said internal clock signal as said receive clock, and in said loopback operation mode, said modulate clock signal as said receive clock, and wherein said clock supply select circuit supplies to said transmitter, in each of said normal operation mode and said loopback operation mode, said internal clock signal as said transmit clock.

Mak teaches of a testing mode provided for self testing of the transmitter and receiver pair provided on-chip. The testing mode targets each module individually; wherein when one of the two devices is placed under test, the other is used as a tester. When the transmitter is the device under test and the receiver is the tester that receives a transmitted signal from the transmitter, the receiver is used to determine the data eye size with the transmitted signal. When the receiver is the device under test and the transmitter is the tester, the transmitter is used to determine the amount of noise and power loss tolerated by the receiver (Abstract, Figs. 4, 9). The transmitter (#140, Fig.4) and the receiver (#180, Fig.4) are tested at the interfaces individually. In particular,

when one of the two devices is a device under test, the other is used as a tester. For example, to test the transmitter (140), the receiver (180) is used as the tester. Similarly, to test the receiver (180), the transmitter (140) is used as the tester. That is, in accordance with the various exemplary embodiments of this invention, two different types of testing are performed for the transmitter and the receiver (Col 3, Lines 54 – 63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the receiver as tester and the transmitter as DUT (device under test) so as to determine the stress tolerance for both receiver and transmitter individually.

Re claim 6, Anderson teaches of a data compare circuit (Col 5, Lines 7 – 19) includes a buffer circuit (chip level pin-out, Fig.4) receiving said transmit data (Fig.4), and a comparator comparing said transmit data output from said buffer circuit and said receive data from said decoder circuit and generating a signal in accordance with a result of the comparison (see rejection of claim 5). However, Enam and Anderson do not teach of retaining said transmit data inside for a period in accordance with a timing difference between said internal clock signal and said modulate clock signal.

Mak teaches of a pass/fail comparator (#190, Fig.5) that compares the loopback received signal from the receiver (180) against the data stream to the transmitter (140) for any mismatch. Due to the delay through the transmitter, the loopback connections and the receiver, there is a need to adjust for the latency (time difference) so that the

data stream to the transmitter will match with the loopback received signal from the receiver. A latency adjuster (150, buffer circuit) is provided to delay the data stream to the transmitter to match with the loopback received signal from the receiver. That is, since the data stream from the pattern generator (110) may take a long path through the transmitter, the loopback connections to the receiver, and the receiver, the data stream from the pattern generator may have the latency adjusted by the latency adjuster (150) so that the data stream can be compared by the pass/fail comparator (190, comparator) with the received signal. The pass/fail comparator compares for a match between the loopback, received signal from the receiver and the data stream from the pattern generator that has been adjusted for latency (Col 5, Lines 1 – 22).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a latency adjuster to for the latency so that the data stream to the transmitter will match with the loopback received signal from the receiver.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Enam in view of Anderson and in further view of Jeong (US 5,675,584).

Re claim 4, Enam and Anderson teach all the limitations of claim 1 as well as Enam also teaches of the clock generate circuit further generating a plurality of clock signals (#416 – 419, multiphase, Fig.4) having a same frequency as said internal clock signal (REFCLK) and with phases different from each other (multiphase) (Paragraph

0090) and the clock modulate circuit including a counter circuit of which count value changes synchronizing to an external trigger (In multiphase PLL the VCO have a ring oscillator which would provide the counter so as to generate different phases for the clock signals) .

However, Enam and Anderson do not specifically teach of a selector circuit receiving said plurality of clock signals from said clock generate circuit and selectively outputting one of said plurality of clock signals that corresponds to said count value as said modulate clock signal.

Jeong teaches of a clock circuit (#60, Fig.3) used to generate the phase clocks supplied to the serial link system. The clock system includes a phase frequency detector (#64, Fig.3), a charge pump and loop filter (#65), and a series of delay cells (#68). The clock system generates a plurality of clock signals (#68, Fig.3) having a same frequency as said internal clock signal (REF, #70) and with phases different from each other (multiphase) (Col 5, Lines 63 – 67 to Col 6, Lines 1 – 26 and Col 15, Lines 50 - 56). The clock modulate circuit includes a counter circuit of which count value changes synchronizing to an external trigger (ring oscillator), and a selector circuit receiving said plurality of clock signals from said clock generate circuit and selectively outputting one of said plurality of clock signals that corresponds to said count value as said modulate clock signal (Multiplexer, Fig.3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the plurality of multiphase clock signals where a

selector would be used to select the most appropriate clock signal so as to perform the loopback test mode.

Claims 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mak et al in view of Olson et al. (US 6,816,987).

Re claim 8, Mak teaches of a communication apparatus, comprising: a transmitter including an encoder circuit (#141, Fig.2) converting transmit data into a transmit signal synchronizing to said clock signal (#140, Figs.1 and 2); a receiver including a decoder circuit (#185, Fig.3) converting a receive signal into receive data synchronizing to said clock signal (Figs 1 and 3, Col 1, Lines 30 - 65).

However, Mak does not specifically teach of a clock generate circuit generating a plurality of clock signals having a same frequency as said clock signal and with phases different from each other and a jitter measure circuit measuring, in a loopback operation mode, jitter occurring in said transmitter, based on a transition of a result of phase comparison between a transition edge of said receive signal and a transition edge of each of said plurality of clock signals.

Olson teaches of an apparatus and method for performing a built-in self-test (BIST) of a data communications system. The apparatus includes a transmitter, a receiver coupled to the transmitter and a test control system coupled to the transmitter and receiver for measuring a data error rate of the data communications system

(Abstract). A sampling system is disclosed, used to determine the amount of timing jitter present in a signal received by the data communications system (Fig.14). The sampling system includes a sampler that uses a multiphase clock (#1408, Fig.14) to generate N samples per data bit period from the data channel (#1409, Fig.14). The digital data has certain maximum levels of skew and jitter. The N samples are sent to sample selector (#1403), which analyzes the samples to determine the optimum sample to be used to recover the original data stream. Multiplexer (#1406) is used to select whichever one of the N samples needs to be sent to BERT 1407 for computation of the bit error rate. As the optimum sampling position moves to the left or to the right of the initial optimum, the BERT continues its computations until enough data has been analyzed. After repeating the BER analysis, a sufficient amount of data will be available to generate a graph (Fig. 15) (Col 13, Lines 15 – 60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a multiphase clock generator that generates multiple clock phases and a jitter measure circuit to determine the amount of timing jitter present for each clock phase in a loopback test mode.

Re claim 9, Olson teaches of the jitter measure circuit (as discussed above in claim 8) that includes a clock sampling circuit detecting each level of said plurality of clocks at each of said transition edges of said receive signal (sampling system, Fig.14), and a phase compare circuit converting a transition of the level of said plurality of clocks

between each of said transition edges of said receive signal, detected by said clock sampling circuit, into a phase difference (Col 13, Lines 58 – 61).

Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mak et al in view of Olson et al and further in view of Yamaguchi et al ("*A new method for testing Jitter tolerance of SerDes devices using sinusoidal jitter*", Advantest Laboratories, University of Washington, Advantest Corporation, Agere Systems, 2002 IEEE).

Mak and Olson teach all the limitations of claim 10 except of a detect signal indicating whether said phase difference obtained by converting the transition of the level of said plurality of clocks exceeds a prescribed jitter tolerance value.

Yamaguchi teaches of a method for measuring jitter tolerance of a SerDes receiver (Abstract). Yamaguchi teaches of a phase compare circuit generating a detect signal indicating whether said phase difference obtained by converting the transition of the level of said plurality of clocks exceeds a prescribed jitter tolerance value (Page 720, Col 1, Figs.3 - 5, equation 18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a jitter tolerance threshold to determine the linear region of the jitter.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mak and Olson as applied to claim 8 above, and further in view of Anderson.

Mak and Olson teach all the limitations of claim 8, except of a differential transmission medium and a signal switch bypassing the differential medium.

Anderson teaches of said transmitter further including a differential driver (#61, Fig.5) converting said transmit signal of a single-end signal into a differential signal to be output, and wherein said receiver further includes a differential receiver (#61, Fig.5) converting a received differential signal into said receive signal of a single-end signal; said communication apparatus further comprising a signal switch (MUX, #55) forming as necessary, in said loopback operation mode, a signal path bypassing said differential driver and said differential receiver for passing said transmit signal output from said encoder circuit directly as said receive signal (Fig. 5. Col 4, Lines 34 – 67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a differential driver in order to achieve cabled communications and a switch to internally bypass the differential driver and set the system into a loopback mode.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al in view of Aronson et al (US Pub 20040076119).

Ramamurthy teaches all the limitations of claim 12 except of a second test mode.

Aronson teaches of a transceiver module having integrated eye diagram opening functionality for reducing jitter is described. The transceiver module may include a transmitter eye opener and a receiver eye opener integrated in single circuit. The transceiver module may also include serial control and various other integrated components. Other functionalities that may be integrated on the transceiver module include loopback modules, bypass features, bit error rate testing, and power down modes (Abstract). Aronson teaches of a second test mode (second loopback) that is different from said first test mode (first loopback) and a normal operation mode (normal operation, Paragraph 0077), said signal switch of said communication apparatus forms a signal path between said communication node and said receive node of said communication apparatus (Paragraph 0069, Fig.9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used multimode loopbacks to allow monitoring the data path integrity at different levels on the transceiver module.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al in view of Enam et al and further in view of Anderson et al.

Ramamurthy teaches all the limitations of claim 12, except of the clock modulation circuit and the clock supply select circuit.

Enam teaches of a communication apparatus, comprising: a transmitter (Fig.3A) including an encoder circuit (MUX, #384, Fig.3A) for converting transmit data (TPDAT, parallel data) into a transmit signal (TSDAT, serial data) synchronizing to a transmit clock (#362); a receiver (Fig.3B) including a decoder circuit (#306 and #310) for converting a receive signal (RSDAT, serial data, Fig.3B) into receive data (RPDAT, parallel data) synchronizing to a receive clock (REFCLK, Fig.3B, Fig.3A); and a clock supply select circuit (#386, Fig.3A) controlling a supply of said transmit clock and said receive clock to said transmitter and said receiver, said clock supply select circuit including a clock generate circuit generating an internal clock signal (Paragraph 0065), and a clock circuit generating a clock signal (#326, Fig.3A, 3B) based on said internal clock of reference (REFCLK), wherein in a normal operation mode, said clock supply select circuit supplies said internal clock signal as each of said transmit clock and said receive clock in common (REFCLK, REFCLK always used in the receiver circuit), and in a loopback operation mode (LLB, #386), said clock supply select circuit supplies said internal clock signal as one of said transmit clock and said receive clock and supplies said modulate clock signal as the other of said transmit clock and said receive clock (Abstract). However, Enam does not teach of a clock modulating circuit that introduces jitter into the internal clock of reference.

Anderson teaches of a circuit for testing jitter tolerance of a receiver. The circuit includes a jitter injection circuit that has an output connected to an input in a phase-locked loop circuit. The jitter injection circuit generates an output signal in response to an application of an input signal. The phase-locked loop circuit has an output that

generates a clock signal, wherein the clock signal may be altered by the output signal from the jitter injection circuit. The clock signal from the phase-locked loop circuit controls transmission of data at the transmitter. Alteration of the clock signal caused by the jitter injection circuit alters the manner in which the transmitter transmits data (Abstract, #13, Fig.5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have introduced jitter into the signal so as to monitor the device response and the tolerance of the receiver line to jitter can be independently tested.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al as applied to claim 12, in view of Olson et al.

Ramamurthy teaches all the limitations of claim 12 as well as a transmitter including an encoder circuit (#11, Fig.3) converting transmit data into a transmit signal synchronizing to said clock signal (#14, Fig.3); a receiver including a decoder circuit (#12, Fig.3) converting a receive signal into receive data synchronizing to said clock signal.

However, Ramamurthy does not specifically teach of a clock generate circuit generating a plurality of clock signals having a same frequency as said clock signal and with phases different from each other and a jitter measure circuit measuring, in a loopback operation mode, jitter occurring in said transmitter, based on a transition of a

result of phase comparison between a transition edge of said receive signal and a transition edge of each of said plurality of clock signals.

Olson teaches of an apparatus and method for performing a built-in self-test (BIST) of a data communications system. The apparatus includes a transmitter, a receiver coupled to the transmitter and a test control system coupled to the transmitter and receiver for measuring a data error rate of the data communications system (Abstract). A sampling system is disclosed, used to determine the amount of timing jitter present in a signal received by the data communications system (Fig.14). The sampling system includes a sampler that uses a multiphase clock (#1408, Fig.14) to generate N samples per data bit period from the data channel (#1409, Fig.14). The digital data has certain maximum levels of skew and jitter. The N samples are sent to sample selector (#1403), which analyzes the samples to determine the optimum sample to be used to recover the original data stream. Multiplexer (#1406) is used to select whichever one of the N samples needs to be sent to BERT 1407 for computation of the bit error rate. As the optimum sampling position moves to the left or to the right of the initial optimum, the BERT continues its computations until enough data has been analyzed. After repeating the BER analysis, a sufficient amount of data will be available to generate a graph (Fig. 15) (Col 13, Lines 15 – 60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a multiphase clock generator that generates multiple clock phases and a jitter measure circuit to determine the amount of timing jitter present for each clock phase in a loopback test mode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER